MF1112-02

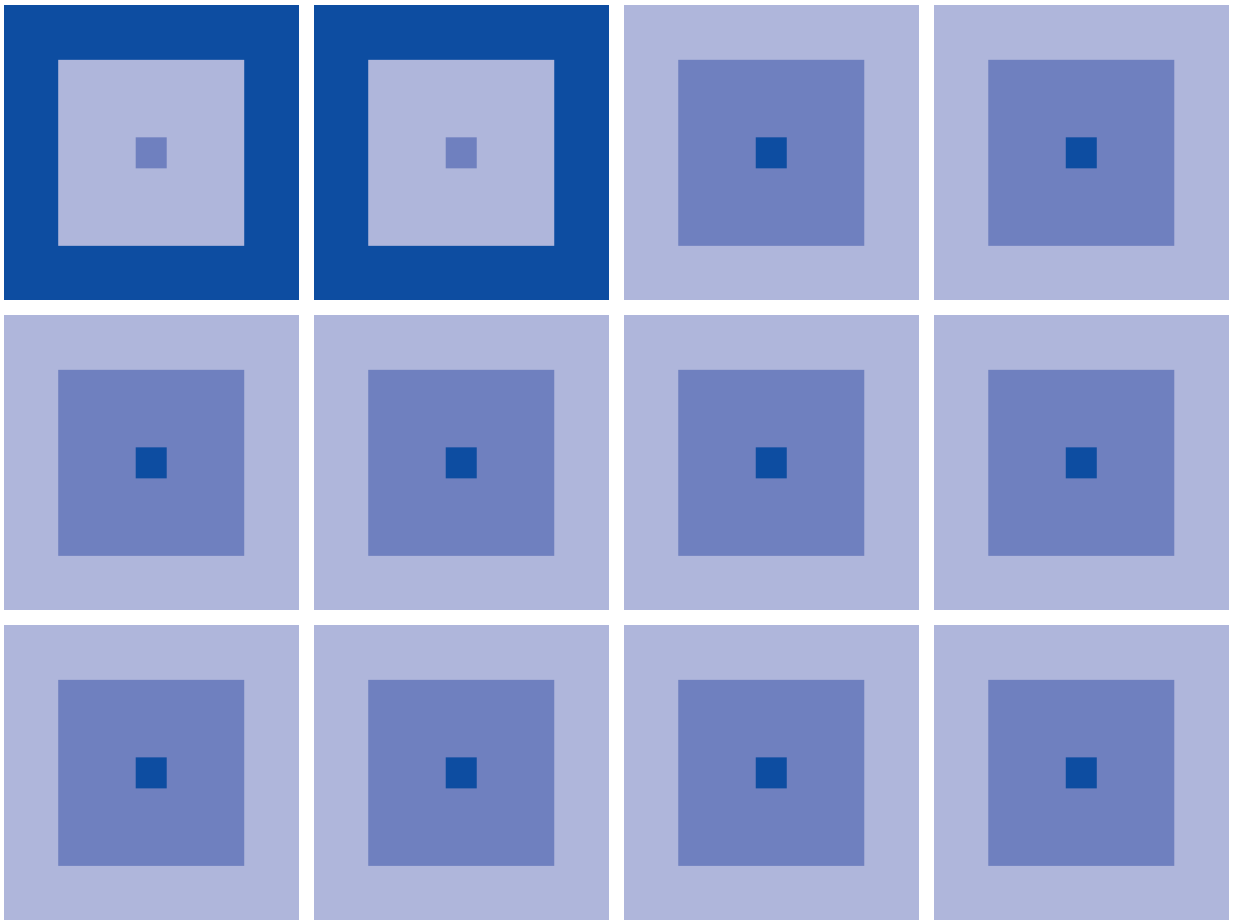
EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C60N04

Technical Manual

S1C60N04 Technical Hardware



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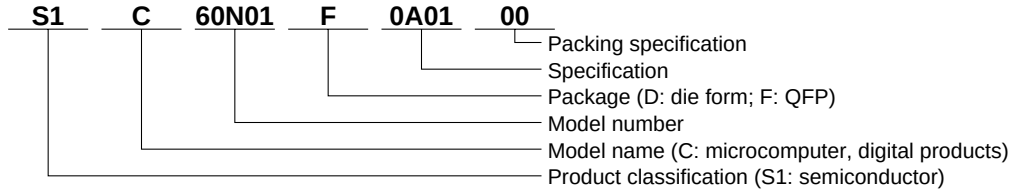
The information of the product number change

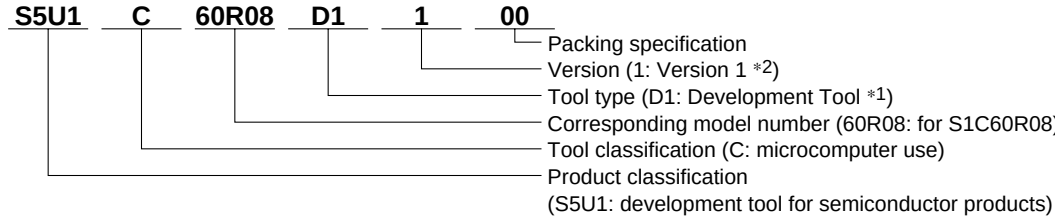
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K

CONTENTS

CHAPTER 1 INTRODUCTION

The S1C60N04 is a single-chip microcomputer which uses an S1C6200B CMOS 4-bit CPU as the core. It contains a 1,536 (words) × 12 (bits) ROM, 144 (words) × 4 (bits) RAM, LCD driver, 4-bit input port (K00–K03), 4-bit output port (R00–R03), 4-bit I/O port (P00–P03) and a timer.

1.1 Features

Core CPU S1C6200B

Built-in oscillation circuit ..... CR oscillation circuit, 2 MHz (Typ.) (V_{SS} = -5 V)

Instruction set ..... 100 instructions

ROM capacity ..... 1,536 words × 12 bits

RAM capacity ..... 144 words × 4 bits

Input port ..... 4 bits (pull-down resistors are available by mask option)

Output ports ..... 4 bits (clock and buzzer outputs are possible by mask option)
R03 output port drivability: 15 mA (V_{SS} = -4.5 V)

I/O port ..... 4 bits

LCD driver ..... 26 segments × 4, 3 or 2 commons
(1/4, 1/3 or 1/2 duty are selectable by mask option)

Timer ..... 1 system built-in

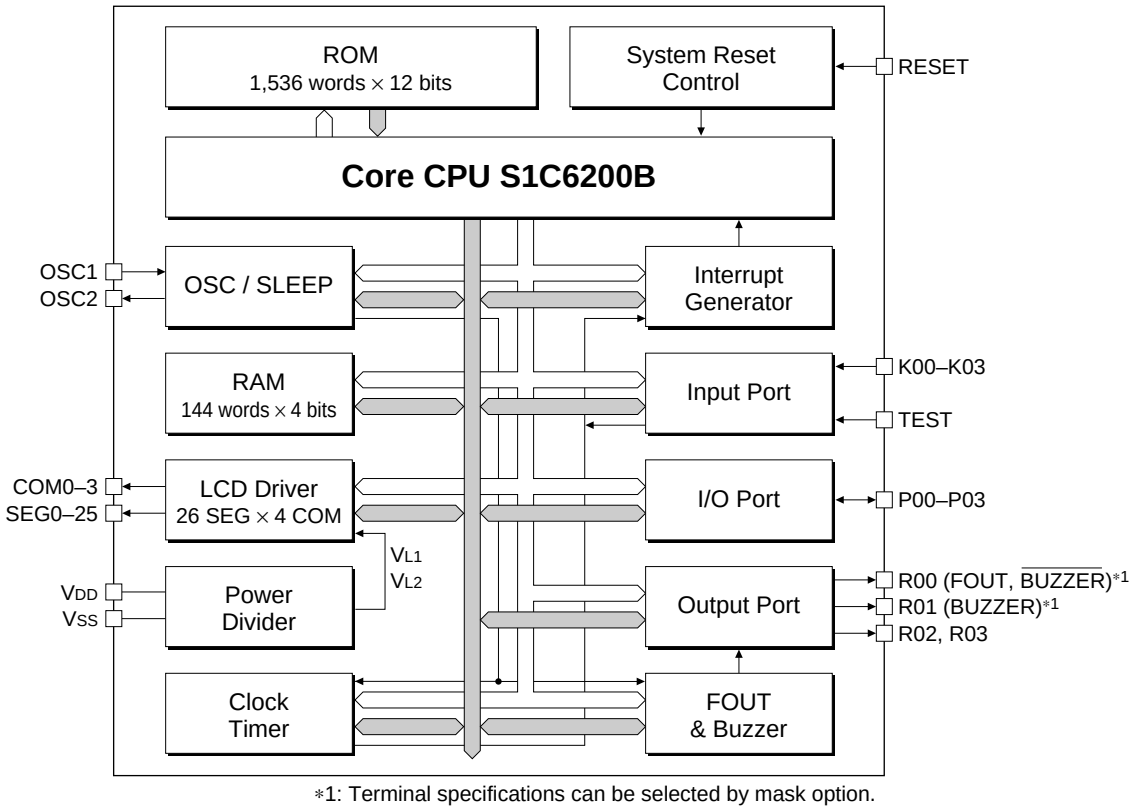
Interrupt ..... External: Input port interrupt 1 system
Internal: Timer interrupt 1 system

Supply voltage ..... 2.7 V to 3.6 V, 4.5 V to 5.5 V

Current consumption (Typ.) ..... During SLEEP: 100 nA (3 V)
100 nA (5 V)
During HALT: 330 µA (3 V)
(LCD ON) 1000 µA (5 V)
During operation: 450 µA (3 V)
(LCD ON) 1100 µA (5 V)

Supply form ..... Die form or QFP12-48pin plastic package

1.2 Block Diagram

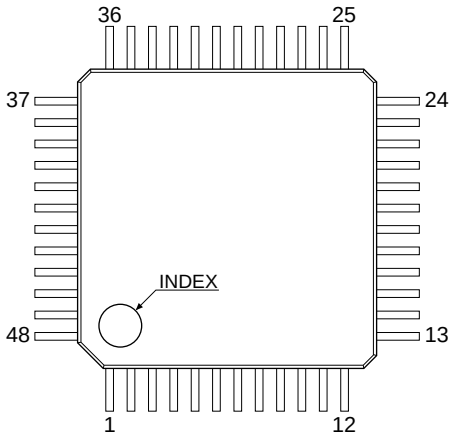


∗1: Terminal specifications can be selected by mask option.

Fig. 1.2.1 S1C60N04 block diagram

1.3 Pin Layout

QFP12-48pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	K02	13	SEG24	25	SEG12	37	SEG0
2	K01	14	SEG23	26	SEG11	38	COM0
3	K00	15	SEG22	27	SEG10	39	COM1
4	P03	16	SEG21	28	SEG9	40	COM2
5	P02	17	SEG20	29	SEG8	41	COM3
6	P01	18	SEG19	30	SEG7	42	TEST
7	P00	19	SEG18	31	SEG6	43	RESET
8	R03	20	SEG17	32	SEG5	44	VDD
9	R02	21	SEG16	33	SEG4	45	OSC1
10	R01	22	SEG15	34	SEG3	46	OSC2
11	R00	23	SEG14	35	SEG2	47	VSS
12	SEG25	24	SEG13	36	SEG1	48	K03

Fig. 1.3.1 S1C60N04 pin layout (QFP12-48pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function
VDD	44	(I)	Power supply pin (+)
VSS	47	(I)	Power supply pin (-)
OSC1	45	I	CR oscillation input pin
OSC2	46	O	CR oscillation output pin
K00–K03	3–1, 48	I	Input port pin
P00–P03	7–4	I/O	I/O port pin
R00	11	O	Output port pin, $\overline{\text{BUZZER}}$ or FOUT output pin *
R01	10	O	Output port pin or BUZZER output pin *
R02, R03	9, 8	O	Output port pin
SEG0–25	37–12	O	LCD segment output pin or DC output pin *
COM0–3	38–41	O	LCD common output pin (1/4 duty, 1/3 or 1/2 duty are selectable *)
RESET	43	I	Initial reset input pin
TEST	42	I	Input pin for test

* Can be selected by mask option

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*) supplied to VDD through VSS, the S1C60N04 generates the necessary internal voltages with the power divider.

* Supply voltage: 2.7 to 3.6 V or 4.5 V to 5.5 V

The power divider generates the LCD drive voltages <VL1, VL2> by dividing the supply voltage as shown in Figure 2.1.1.
The circuit configuration is set according to the LCD drive bias selection with a mask option.
When 1/3 bias is selected, the supply voltage is divided by 3 to generate VL1 and VL2.
When 1/2 bias is selected, the supply voltage is divided by 2 and VL1 and VL2 is shorted internally.

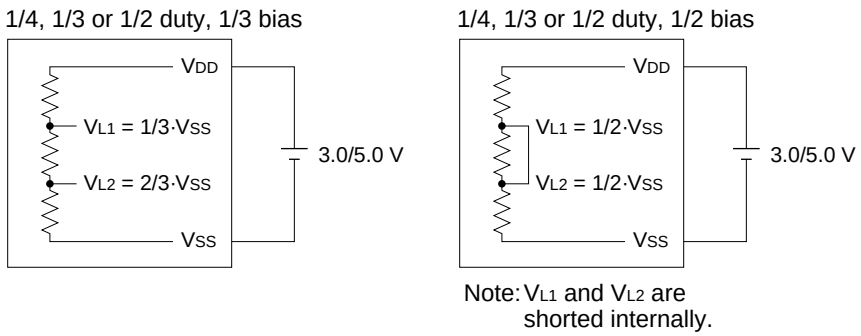


Fig. 2.1.1 Configuration of power divider

2.2 Initial Reset

To initialize the S1C60N04 circuits, an initial reset must be executed. There are three ways of doing this.

(1) Initial reset by the power-on reset circuit
(2) External initial reset via the RESET pin
(3) External initial reset by simultaneous high input to pins K00–K03 (depending on mask option)

Figure 2.2.1 shows the configuration of the initial reset circuit.

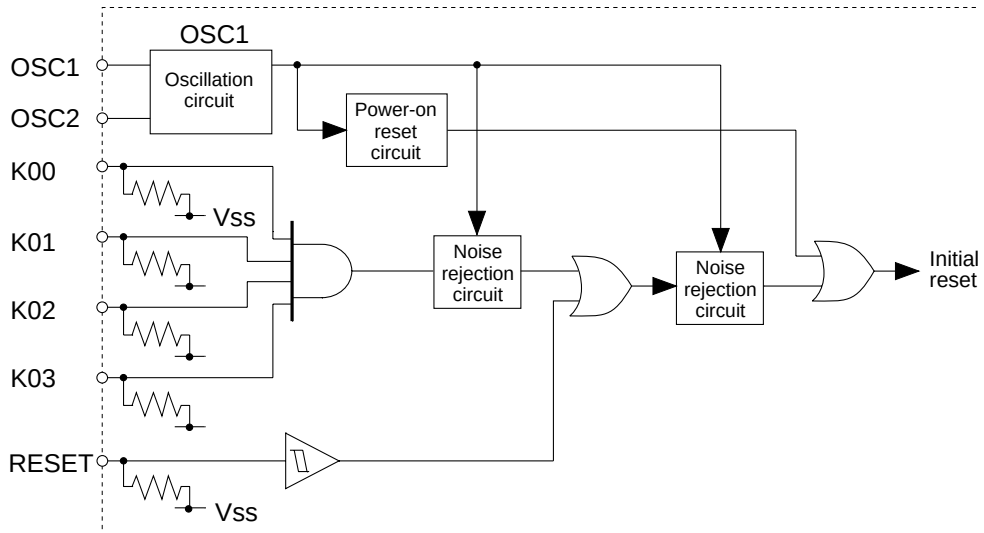


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Power-on reset circuit

The power-on reset circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating.

Note: The power-on reset circuit may not work properly due to unstable or lower voltage input. The following two initial reset method are recommended to generate the initial reset signal.

2.2.2 Reset pin (RESET)

An initial reset can be invoked externally by making the reset pin high.
When the reset pin goes low the CPU begins to operate.

2.2.3 Simultaneous high input to input ports (K00–K03)

Another way of invoking an initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port pins must be kept high for at least 1 sec (when oscillating frequency fosc = 2 MHz), tolerance is within 5%, because of the noise rejection circuit. Table 2.2.3.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.3.1 Input port combinations

A	Not used
B	K00*K01
C	K00*K01*K02
D	K00*K01*K02*K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

When this function is used, make sure that the specified ports do not go high at the same time during normal operation.

2.2.4 Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.4.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	144×4	Undefined
Display memory	26×4	Undefined
Other peripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.3 Test Pin (TEST)

This pin is used when IC is inspected for shipment. During normal operation connect it to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C60N04 employs the S1C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the S1C6200 / 6200A / 6200B.
Refer to the "S1C6200 / 6200A Core CPU Manual" for details of the S1C6200B, which is compatible with the S1C6200A.

Note the following points with regard to the S1C60N04:

(1) Since the S1C60N04 provides the SLEEP function, the SLP instruction can be used.

(2) Because the ROM capacity is 1,536 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

```
PUSH XP    POP XP    LD XP,r    LD r,XP
PUSH YP    POP YP    LD YP,r    LD r,YP
```

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of 1,536 × 12-bit steps. The program area is 6 pages (0–5), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is set to page 1, step 00H. The interrupt vectors are allocated to page 1, steps 01H–07H.

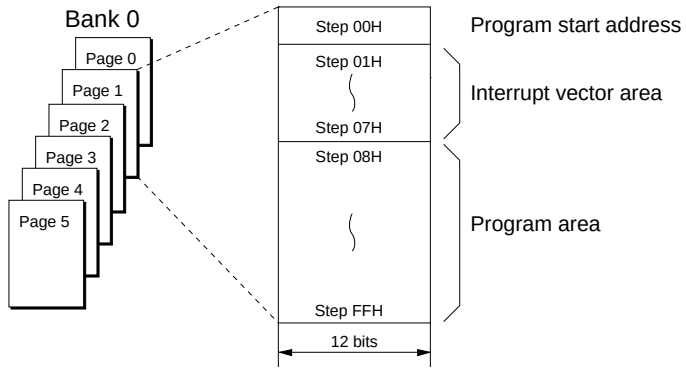


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 144 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C60N04 are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the S1C60N04 has an address space of 188 words, of which 32 words are allocated to display memory and 12 words, to I/O memory. Figure 4.1.1 show the overall memory map for the S1C60N04, and Table 4.1.1, the memory maps for the peripheral circuits (I/O space).

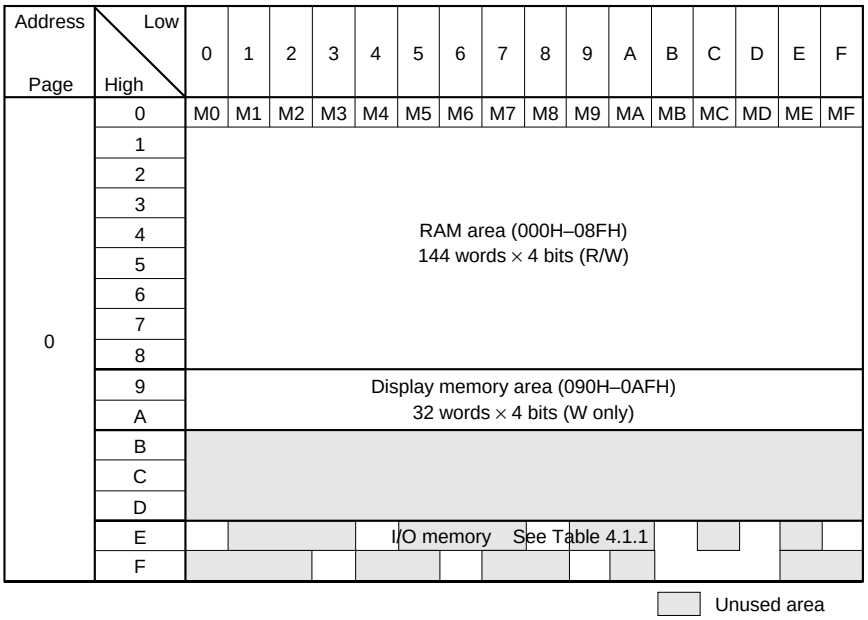


Fig. 4.1.1 Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0E4H	TM3	TM2	TM1	TM0	TM3	– *2			Clock timer data (2 Hz)
					TM2	– *2			Clock timer data (4 Hz)
	R				TM1	– *2			Clock timer data (8 Hz)
					TM0	– *2			Clock timer data (16 Hz)
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F3H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data
					R02	0	High	Low	R02 output port data
			BUZZER	FOUT	R01	0	High	Low	R01 output port data
				BUZZER	BUZZER	0	On	Off	Buzzer output On/Off control
	R/W				R00	0	High	Low	R00 output port data
					FOUT	0	On	Off	FOUT output On/Off control
					$\overline{\text{BUZZER}}$	0	On	Off	Buzzer inverted output On/Off control
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0F9H	0	TMRST	0	0	0 *3	– *2	–	–	Unused
					TMRST*3	Reset	Reset	–	Clock timer reset
	R	W	R		0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
0FBH	0	0	0	PDON	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					PDON	0	On	Off	LCD power supply On/Off control
0FCH	0	0	0	IOC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					IOC	0	Output	Input	I/O port I/O control
0FDH	XBZR	0	0	0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
					0 *3	– *2	–	–	Unused
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Always "0" being read

*4 Reset (0) immediately after being read

4.2 Oscillation Circuit

The S1C60N04 has a CR oscillation circuit.
The CR oscillation circuit generates the operating clock for the CPU and the peripheral circuits. The oscillation frequency is 2 MHz (Typ.). Figure 4.2.1 is the circuit diagram of the CR oscillation circuit.

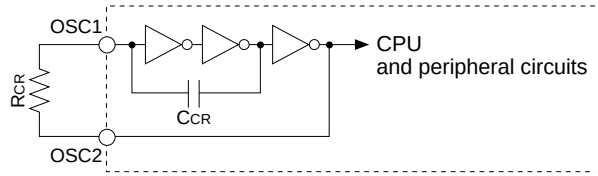


Fig. 4.2.1 CR oscillation circuit

As shown in Figure 4.2.1, the CR oscillation circuit can be configured simply by connecting the resistor RCR between the OSC1 and OSC2 terminals.
See Chapter 6, "Electrical Characteristics" for resistance value of RCR.

4.3 Input Ports (K00–K03)

4.3.1 Configuration of input port

The S1C60N04 has a 4-bit general-purpose input port. Each of the input port pins (K00–K03) has an internal pull-down resistor. The pull-down resistor can be selected for each bit with the mask option. Figure 4.3.1.1 shows the configuration of input port.

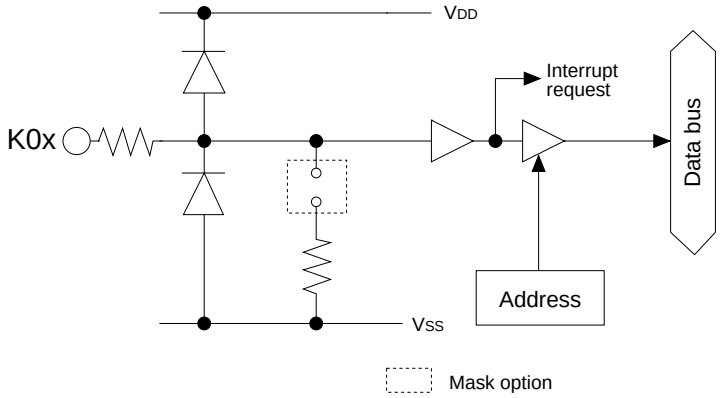


Fig. 4.3.1.1 Configuration of input port

Selecting "pull-down resistor enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.3.2 Interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2.1 shows the configuration of K00–K03.

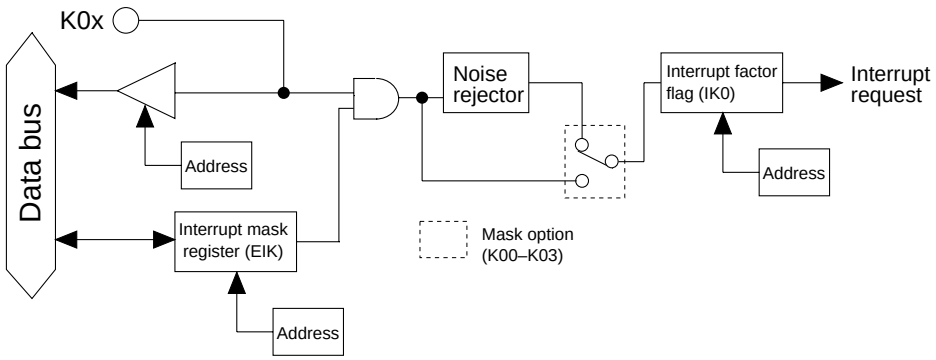
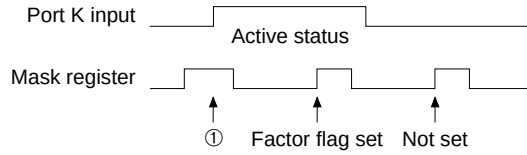


Fig. 4.3.2.1 Input interrupt circuit configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to 1.

Input interrupt programming related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.3.2.2 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = high status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.3.2.2. However, when clearing the content of the mask register with the input terminal kept in the high status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (high status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (low status).

4.3.3 Mask option

The contents that can be selected with the input port mask option are as follows:

(1) An internal pull-down resistor can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-down resistor disabled", take care that the input does not float. Select "pull-down resistor enabled" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring through noise. The mask option enables selection of the noise rejection circuit for each separate pin series. When "use" is selected, a maximum delay of 0.5 msec (fosc = 2 MHz), tolerance is within 5%, occurs from the time an interrupt condition is established until the interrupt factor flag (IK0) is set to 1.

4.3.4 I/O memory of input port

Table 4.3.4.1 list the input port control bits and their addresses.

Table 4.3.4.1 Input port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EDH	0	0	0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

K00–K03: Input port data (0E0H)

The input data of the input port pins can be read with these registers.

When 1 is read: High level
When 0 is read: Low level
Writing: Invalid

The value read is 1 when the pin voltage of the four bits of the input port (K00–K03) goes high (V_{DD}), and 0 when the voltage goes low (V_{SS}). These bits are reading, so writing cannot be done.

EIK00–EIK03: Interrupt mask registers (0E8H)

Masking the interrupt of the input port pins can be done with these registers.

When 1 is written: Enable
When 0 is written: Mask
Reading: Valid

With these registers, masking of the input port bits can be done for each of the four bits. After an initial reset, these registers are all set to 0.

IK0: Interrupt factor flag (0EDH•D0)

This flag indicates the occurrence of an input interrupt.

When 1 is read: Interrupt has occurred
When 0 is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to 0.

4.3.5 Programming note

When modifying the input port from high level to low level with pull-down resistor, a delay will occur at the fall of the waveform due to time constant of the pull-down resistor and input gate capacities. Provide appropriate waiting time in the program when performing input port reading.

4.4 Output Ports (R00–R03)

4.4.1 Configuration of output port

The S1C60N04 has a 4-bit general output port (R00–R03).
Output specification of the output port can be selected in a bit units with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports. Figure 4.4.1.1 shows the configuration of the output port.

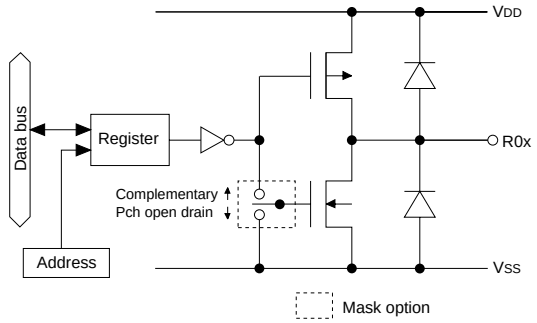


Fig. 4.4.1.1 Configuration of output port

4.4.2 Mask option

The mask option enables the following output port selection.

(1) Output specification of output port

The output specifications for the output port (R00–R03) may be either complementary output or Pch open drain output for each bit. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.2.1. Figure 4.4.2.1 shows the structure of output ports R00–R03.

Table 4.4.2.1 Special output

Output port	Special output
R00	FOUT or $\overline{\text{BUZZER}}$ output
R01	BUZZER output

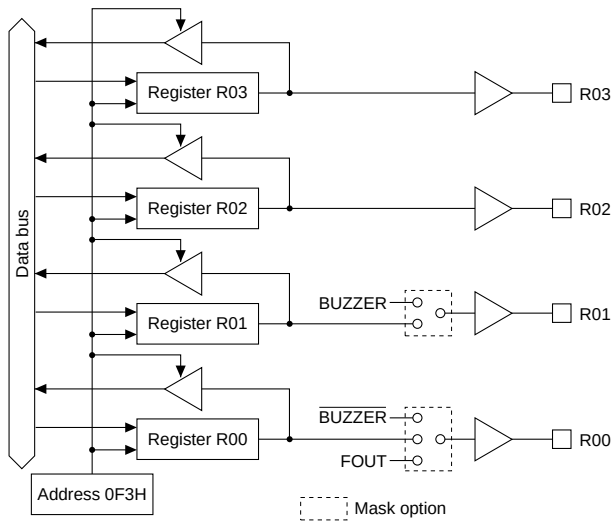


Fig. 4.4.2.1 Structure of output ports R00–R03

FOUT (R00)

When output port R00 is set for FOUT output, this port will generate fosc (CPU operating clock frequency) clock.

BUZZER, $\overline{\text{BUZZER}}$ (R01, R00)

Output ports R01 and R00 may be set to BUZZER output and $\overline{\text{BUZZER}}$ output (BUZZER reverse output), respectively, allowing for direct driving of the piezo-electric buzzer.
$\overline{\text{BUZZER}}$ output (R00) may only be set if R01 is set to BUZZER output. In such case, whether ON / OFF of the $\overline{\text{BUZZER}}$ output is done through R00 register or is controlled through R01 simultaneously with BUZZER output is also selected by mask option.
The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz.

4.4.3 I/O memory of output port

Table 4.4.3.1 lists the output port control bits and their addresses.

Table 4.4.3.1 Control bits of output port

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F3H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data
					R02	0	High	Low	R02 output port data
			BUZZER	FOUT	R01	0	High	Low	R01 output port data
				$\overline{\text{BUZZER}}$	BUZZER	0	On	Off	Buzzer output On/Off control
	R/W				R00	0	High	Low	R00 output port data
					FOUT	0	On	Off	FOUT output On/Off control
					$\overline{\text{BUZZER}}$	0	On	Off	Buzzer inverted output On/Off control
0FDH	XBZR	0	0	0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
					0 *3	– *2	–	–	Unused
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

R00–R03: Output port data (0F3H)

Sets the output data for the output ports.

When 1 is written: High output
When 0 is written: Low output
Reading: Valid

The output port pins output the data written to the corresponding registers (R00–R03) without changing it. When 1 is written to the register, the output port pin goes high (V_{DD}), and when 0 is written, the output port pin goes low (V_{SS}).
After an initial reset, all the registers are set to 0.

R00 (when FOUT is selected): Special output port data (0F3H•D0)

Controls the FOUT (fosc clock) output.

When 1 is written: Clock output
When 0 is written: Low level (DC) output
Reading: Valid

FOUT output can be controlled by writing data to R00.
After an initial reset, this register is set to 0.
Figure 4.4.3.1 shows the output waveform for FOUT output.

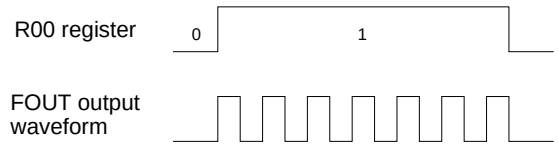


Fig. 4.4.3.1 FOUT output waveform

Note: *A hazard may occur when the FOUT signal is turned ON or OFF.*

R00, R01 (when buzzer output is selected): Special output port data (0F3H•D0, D1)

Controls the buzzer output.

When 1 is written: Buzzer output
When 0 is written: Low level (DC) output
Reading: Valid

$\overline{\text{BUZZER}}$ and BUZZER output can be controlled by writing data to R00 and R01.
When $\overline{\text{BUZZER}}$ output by R01 register control is selected by mask option, BUZZER output and $\overline{\text{BUZZER}}$ output can be controlled simultaneously by writing data to R01 register.
After an initial reset, these registers are set to 0.
Figure 4.4.3.2 shows the output waveform for buzzer output.

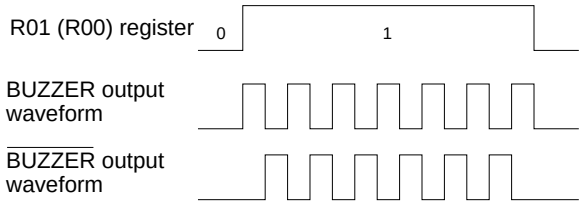


Fig. 4.4.3.2 Buzzer output waveform

Note: *A hazard may occur when the BUZZER or $\overline{\text{BUZZER}}$ signal is turned ON or OFF.*

XBZR: Buzzer frequency control (0FDH•D3)

Selects the frequency of the buzzer signal.

When 1 is written: 2 kHz
When 0 is written: 4 kHz
Reading: Valid

When R00 and R01 port is set to buzzer output, the frequency of the buzzer signal can be selected by this register.
When 1 is written to this register, the frequency is set in 2 kHz, and in 4 kHz when 0 is written.
After an initial reset, this register is set to 0.

4.4.4 Programming note

The buzzer output signal may produce hazards when the output ports R00 and R01 are turned on or off.

4.5 I/O Ports (P00–P03)

4.5.1 Configuration of I/O port

The S1C60N04 has a 4-bit general-purpose I/O port. Figure 4.5.1.1 shows the configuration of the I/O port. The four bits of the I/O port P00–P03 can be set to either input mode or output mode. The mode can be set by writing data to the I/O control register (IOC).

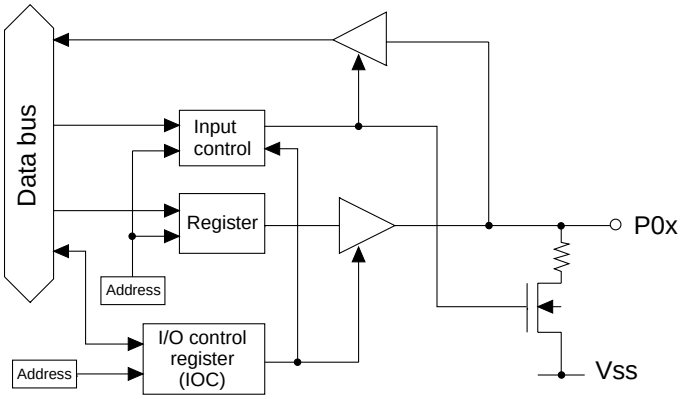


Fig. 4.5.1.1 Configuration of I/O port

4.5.2 I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 by writing data into I/O control register IOC.
To set the input mode, 0 is written to the I/O control register. When an I/O port is set to input mode, its impedance becomes high and it works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when 1 is written to the I/O control register (IOC). When an I/O port set to output mode works as an output port, it outputs a high signal (V_{DD}) when the port output data is 1, and a low signal (V_{SS}) when the port output data is 0.
After an initial reset, the I/O control register is set to 0, and the I/O port enters the input mode.

4.5.3 Mask option

The output specification during output mode (IOC = 1) of the I/O port can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of the I/O port. However, when Pch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

4.5.4 I/O memory of I/O port

Table 4.5.4.1 lists the I/O port control bits and their addresses.

Table 4.5.4.1 I/O port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0FCH	0	0	0	IOC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					IOC	0	Output	Input	I/O port I/O control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

P00–P03: I/O port data (0F6H)

I/O port data can be read and output data can be written through the port.

When writing data

When 1 is written: High level
When 0 is written: Low level

When an I/O port is set to the output mode, the written data is output from the I/O port pin unchanged. When 1 is written as the port data, the port pin goes high (V_{DD}), and when 0 is written, the level goes low (V_{SS}). Port data can also be written in the input mode.

When reading data

When 1 is read: High level
When 0 is read: Low level

The pin voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port pin can be read; in the output mode the output voltage level can be read. When the pin voltage is high (V_{DD}) the port data read is 1, and when the pin voltage is low (V_{SS}) the data is 0. Also, the built-in pull-down resistor functions during reading, so the I/O port pin is pulled down.

IOC: I/O control register (0FCH•D0)

The input or output I/O port mode can be set with this register.

When 1 is written: Output mode
When 0 is written: Input mode
Reading: Valid

The input or output mode of the I/O port is set in units of four bits. For instance, IOC sets the mode for P00–P03.
Writing 1 to the I/O control register makes the I/O port enter the output mode, and writing 0, the input mode.
After an initial reset, the IOC register is set to 0, so the I/O port is in the input mode.

4.5.5 Programming note

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 60 kΩ

4.6 LCD Driver (COM0–COM3, SEG0–SEG25)

4.6.1 Configuration of LCD driver

The S1C60N04 has four common pins and 26 (SEG0–SEG25) segment pins, so that an LCD with a maximum of 104 (26 × 4) segments can be driven. The power for driving the LCD is generated by the CPU internal circuit, so there is no need to supply power externally.
The driving method is 1/4 duty (or 1/3, 1/2 duty by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{DD}, V_{L1}, V_{L2} and V_{SS}. Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{DD}, V_{L1} = V_{L2} and V_{SS}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).
The LCD drive voltages V_{L1} and V_{L2} are generated by the power divider inside the IC. However it is necessary to turn the power divider on by writing 1 to the PDON register before starting LCD display.
The frame frequency is about 30.5 Hz for 1/4 duty and 1/2 duty, and 40.7 Hz for 1/3 duty (in the case of fosc = 2 MHz), tolerance is within 5%.
Figures 4.6.1.1 to 4.6.1.6 show the drive waveform for each duty and bias.

Note: "fosc" indicates the oscillation frequency of the oscillation circuit.

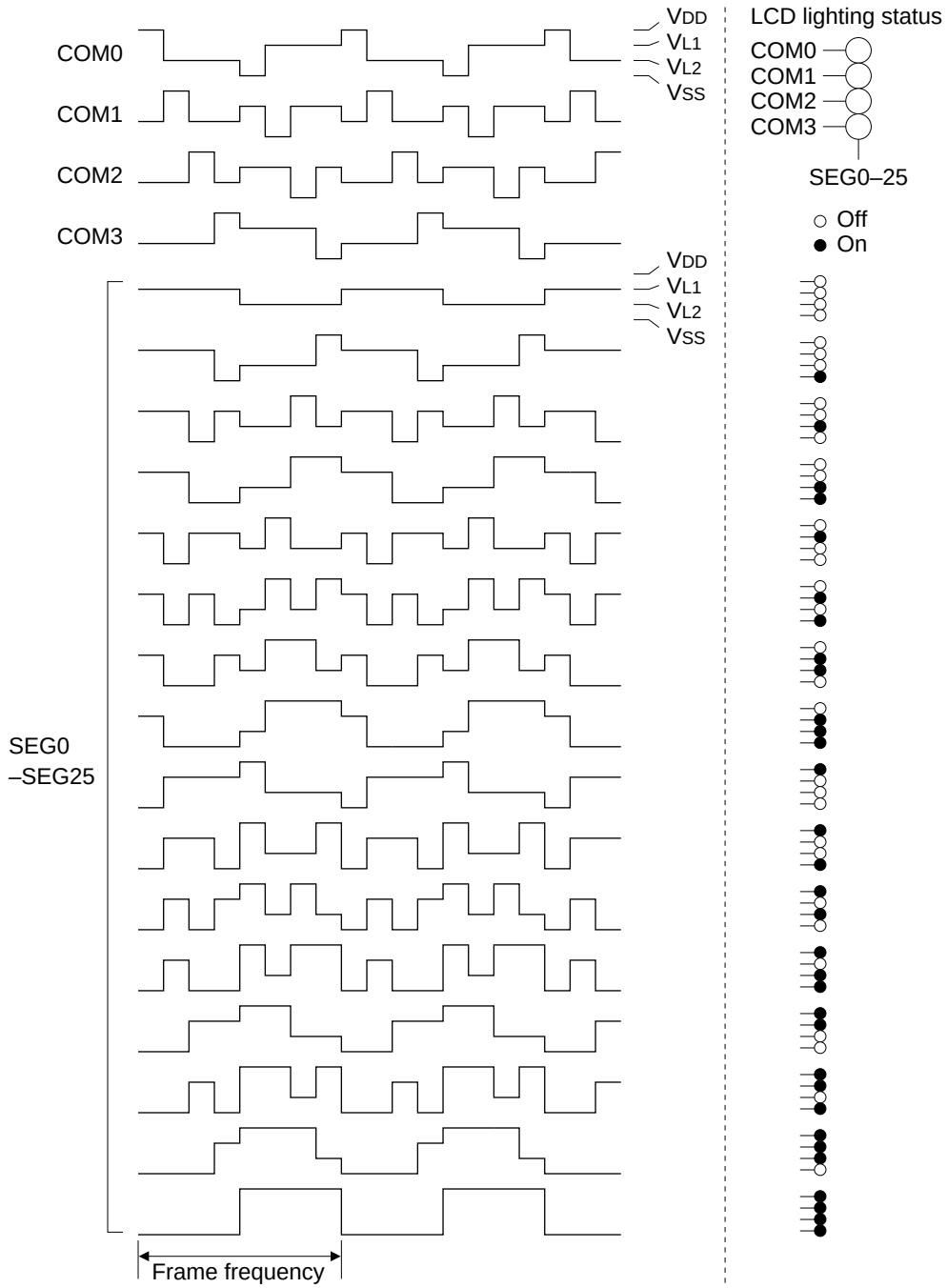


Fig. 4.6.1.1 Drive waveform for 1/4 duty (1/3 bias)

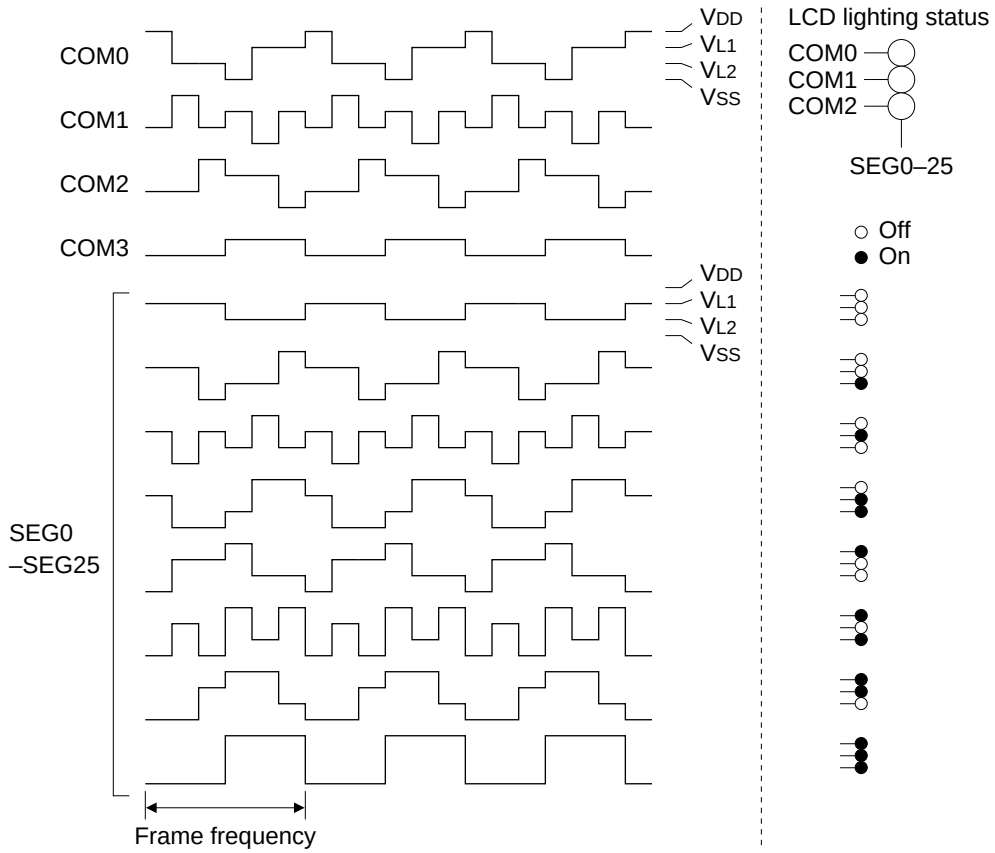


Fig. 4.6.1.2 Drive waveform for 1/3 duty (1/3 bias)

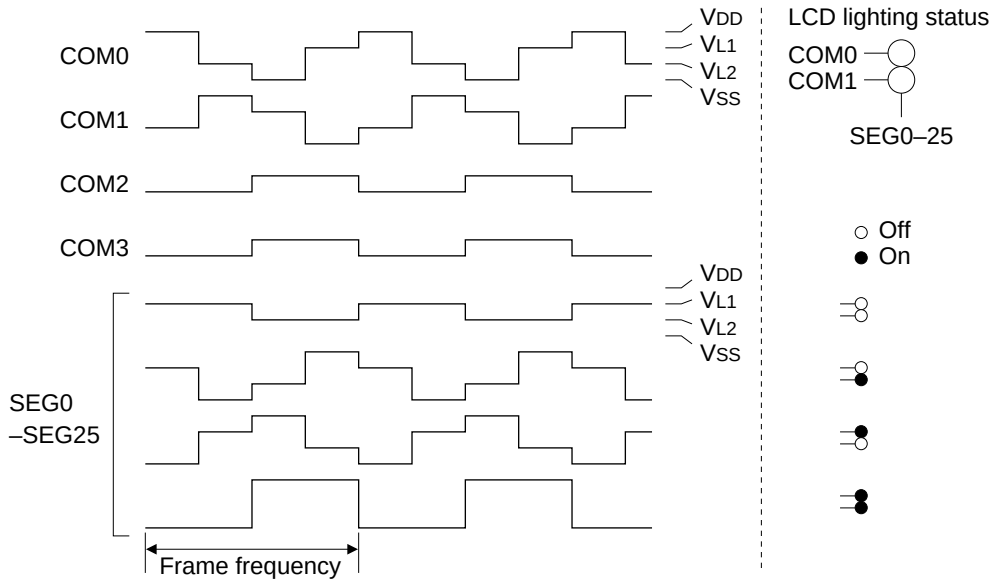


Fig. 4.6.1.3 Drive waveform for 1/2 duty (1/3 bias)

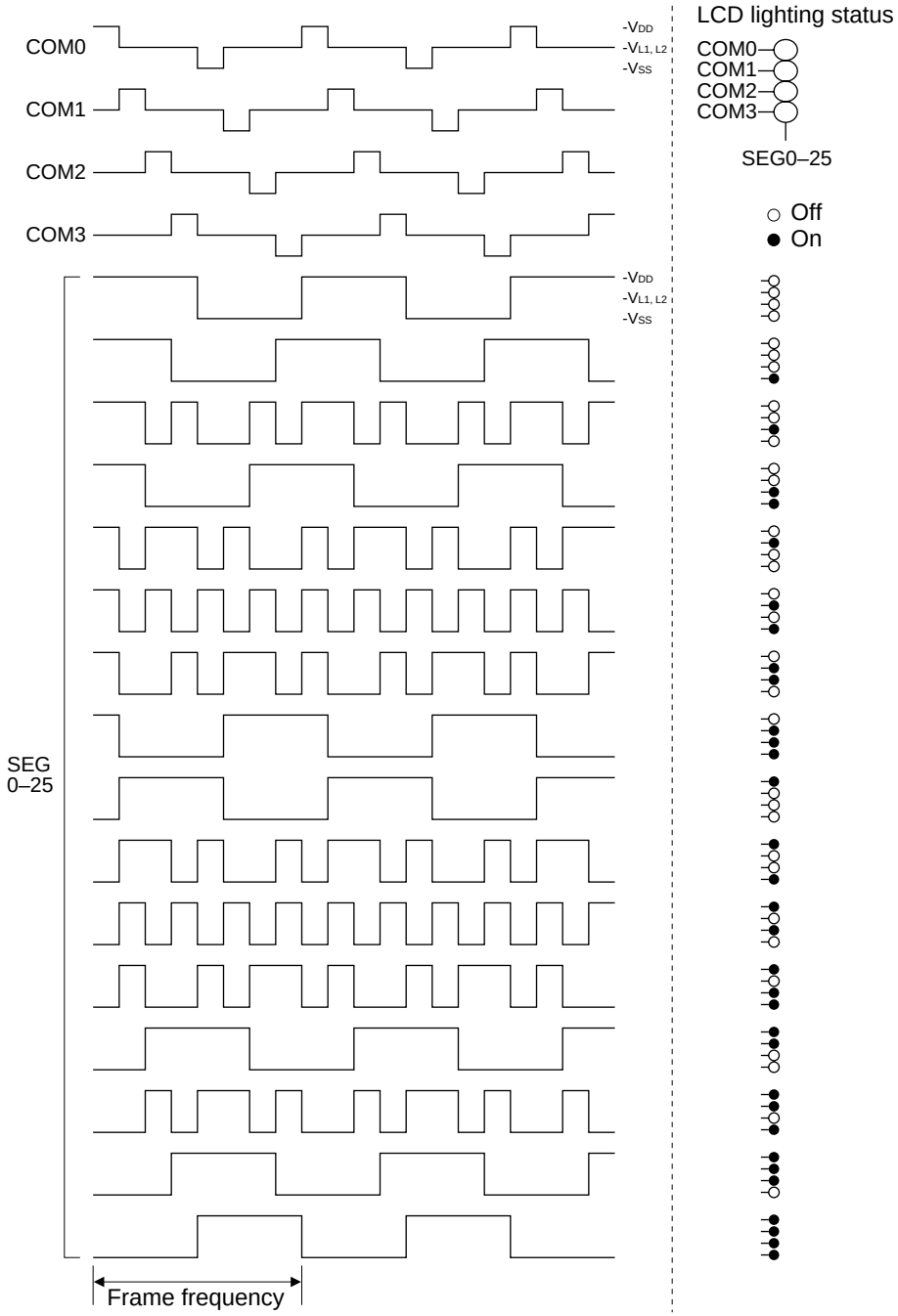


Fig. 4.6.1.4 Drive waveform for 1/4 duty (1/2 bias)

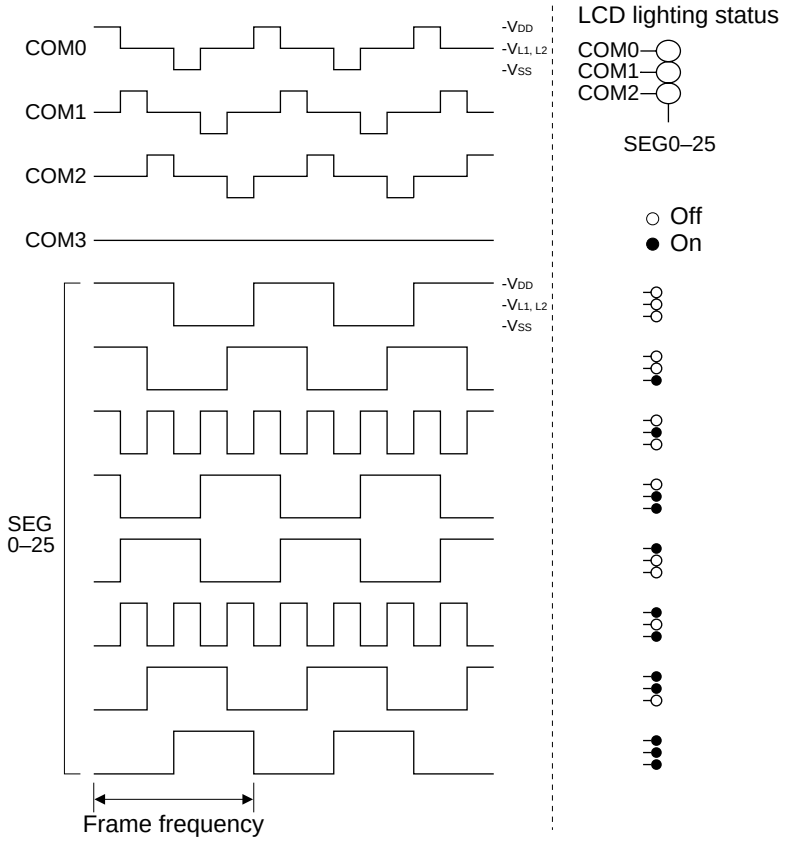


Fig. 4.6.1.5 Drive waveform for 1/3 duty (1/2 bias)

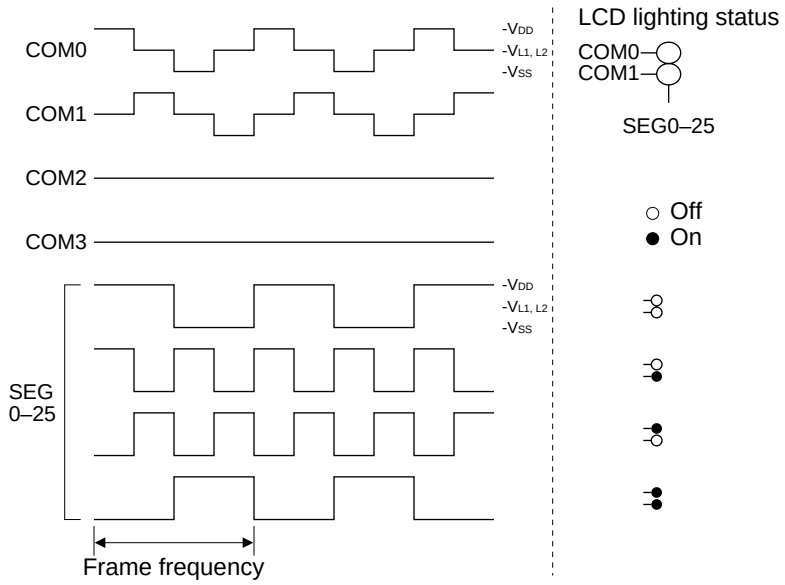


Fig. 4.6.1.6 Drive waveform for 1/2 duty (1/2 bias)

4.6.2 Mask option

(1) Segment allocation

As shown in Figure 4.l.1, the S1C60N04 display data is decided by the data written to the display memory (write-only) at address 090H–0AFH.

The address and bits of the display memory can be made to correspond to the segment pins (SEG0–SEG25) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.2.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
09AH	d	c	b	a
09BH	p	g	f	e
09CH	d'	c'	b'	a'
09DH	p'	g'	f'	e'

Display data memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

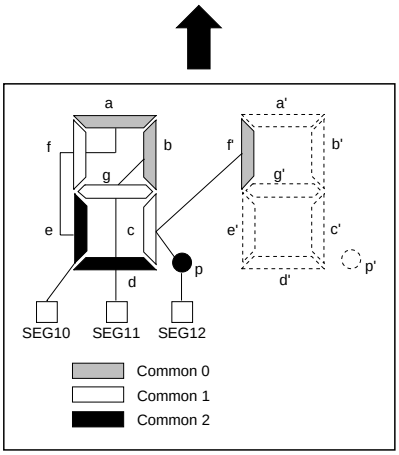


Fig. 4.6.2.1 Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty. Table 4.6.2.1 shows the differences in the number of segments according to the selected duty.

Table 4.6.2.1 Differences according to selected duty

Duty	COM used	Max. number of segments	Frame frequency *
1/4	COM0–COM3	104 (26 × 4)	30.5 Hz
1/3	COM0–COM2	78 (26 × 3)	40.7 Hz
1/2	COM0–COM1	52 (26 × 2)	30.5 Hz

* When fOSC = 2 MHz, tolerance is within 5%

(3) Output specification

① The segment pins (SEG0–SEG25) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment pin is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each pin by mask option.

Note: The pin pairs are the combination of SEG (2∗n) and SEG (2∗n + 1) (where n is an integer from 0 to 12).

(4) Drive bias

For the drive bias of the S1C60N04, either 1/3 bias or 1/2 bias can be selected by the mask option.

4.6.3 I/O memory of LCD driver

Table 4.6.3.1 shows the control bits of the LCD driver and their addresses. Figure 4.6.3.1 shows the display memory map.

Table 4.6.3.1 Control bits of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FBH	0	0	0	PDON	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					PDON	0	On	Off	LCD power supply on/off control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
090	Display memory (Write only) 32 words x 4 bits															
0A0																

Fig. 4.6.3.1 Display memory map

PDON: LCD power supply On/Off control (0FBH•D0)

Controls the power supply for LCD display.

When 1 is written: LCD power On
When 0 is written: LCD power Off
Reading: Valid

By writing 1 to PDON, the LCD display can work normally. When 0 is written, all the segment and common signals will go to the same voltage level, and the LCD display goes off.
This control dose not affect the contents of display memory.
After an initial reset, this register is set to 0.

Display memory (090H–0AFH)

The LCD segments are turned on or off according to this data.

When 1 is written: On
When 0 is written: Off
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off.
After an initial reset, the contents of the display memory are undefined.

4.6.4 Programming note

Because the display memory is for writing only, re-writing the contents with computing instructions (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.

4.7 Clock Timer

4.7.1 Configuration of clock timer

The S1C60N04 has a built-in clock timer that uses the oscillation circuit as the clock source. The clock timer is configured as a 7-bit binary counter that counts with a 256 Hz source clock from the divider. The high-order 4 bits of the counter (16 Hz–2 Hz) can be read by the software.
Figure 4.7.1.1 is the block diagram of the clock timer.

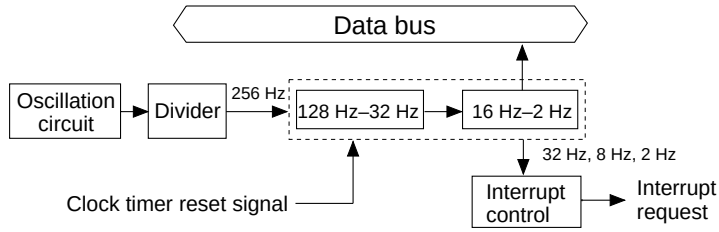


Fig. 4.7.1.1 Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

4.7.2 Interrupt function

The clock timer can generate interrupts at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.
Figure 4.7.2.1 is the timing chart of the clock timer.

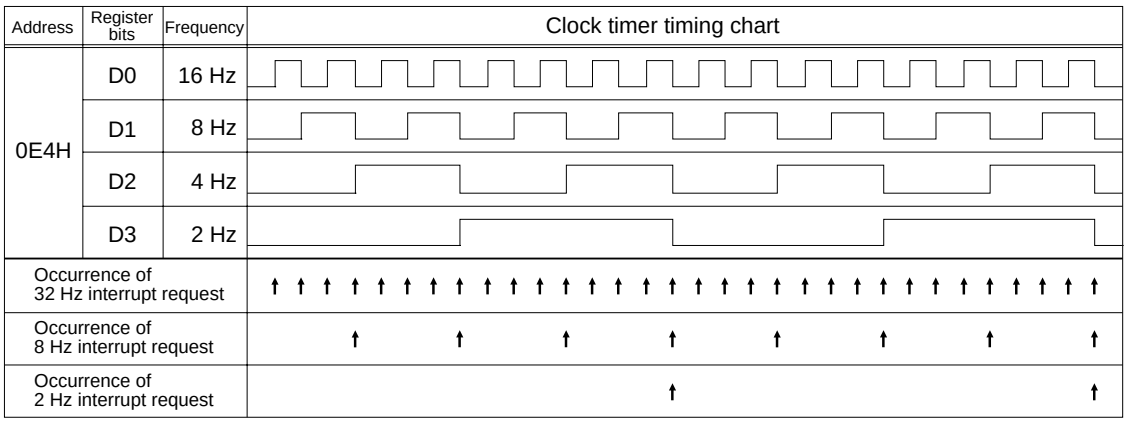


Fig. 4.7.2.1 Timing chart of the clock timer

As shown in Figure 4.7.2.1, an interrupt is generated at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. At this point, the corresponding interrupt factor flag (IT32, IT8, IT2) is set to 1. The interrupts can be masked individually with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flags will be set to 1 at the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to 1).

4.7.3 I/O memory of clock timer

Table 4.7.3.1 shows the clock timer control bits and their addresses.

Table 4.7.3.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E4H	TM3	TM2	TM1	TM0	TM3	– *2			Clock timer data (2 Hz)
					TM2	– *2			Clock timer data (4 Hz)
	R				TM1	– *2			Clock timer data (8 Hz)
					TM0	– *2			Clock timer data (16 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F9H	0	TMRST	0	0	0 *3	– *2	–	–	Unused
					TMRST*3	Reset	Reset	–	Clock timer reset
	R	W	R		0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

TM0–TM3: Timer data (0E4H)

The l6 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.
At initial reset, the timer data is initialized to "0H".

EIT32, EIT8, EIT2: Interrupt mask registers (0EBH•D0–D2)

These registers are used to mask the clock timer interrupt.

When 1 is written: Enabled
When 0 is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to 0.

IT32, IT8, IT2: Interrupt factor flags (0EFH•D0–D2)

These flags indicate the status of the clock timer interrupt.

When 1 is read: Interrupt has occurred
When 0 is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to 1 at the falling edge of the signal. These flags can be reset when the register is read by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to 0.

TMRST: Clock timer reset (0F9H•D2)

This bit resets the clock timer.

When 1 is written: Clock timer reset
When 0 is written: No operation
Reading: Always 0

The clock timer is reset by writing 1 to TMRST. The clock timer starts immediately after this. No operation results when 0 is written to TMRST.
This bit is write-only, and so is always 0 when read.

4.7.4 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the oscillation frequency is not 2 MHz. In the case of S1C60N04, tolerance is within 5%.

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.8 Interrupt and HALT/SLEEP

Interrupt types

The S1C60N04 provides the following interrupt settings, each of which is maskable.

External interrupt: Input port interrupt (one)
Internal interrupt: Timer interrupt (one)

To enable interrupts, the interrupt flag must be set to 1 (EI) and the necessary related interrupt mask registers must be set to 1 (enable). When an interrupt occurs, the interrupt flag is automatically reset to 0 (DI) and interrupts after that are inhibited.
Figure 4.8.1 shows the configuration of the interrupt circuit.

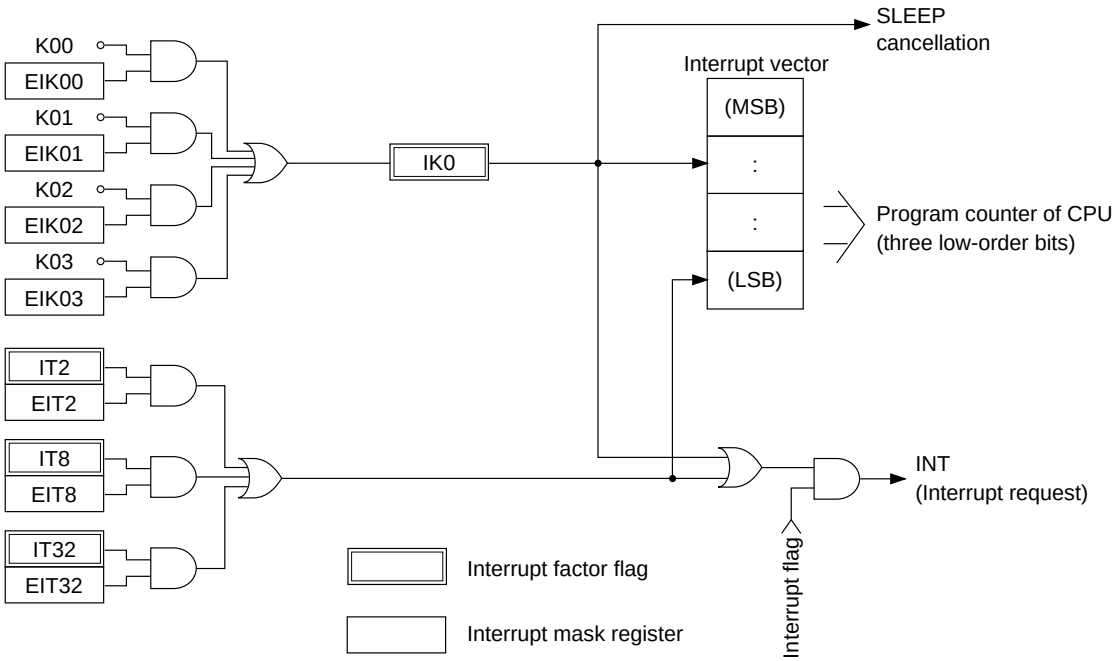


Fig. 4.8.1 Configuration of interrupt circuit

HALT and SLEEP modes

When the HALT instruction is executed, the CPU stops operating and enters the HALT mode. The oscillation circuit and the peripheral circuits operate in the HALT mode. By an interrupt, the CPU exits the HALT mode and resumes operating.

Executing the SLP instruction set the IC in the SLEEP mode that stops operations of the CPU and oscillation circuit. The SLEEP mode will be canceled by an input interrupt request from the input port K00–K03. Consequently, at least one input port (K00, K01, K02 or K03) interrupt must be enabled before shifting to the SLEEP status. When the SLEEP status is canceled by a K0n input interrupt, the CPU waits for oscillation to stabilize then restarts operating.

Refer to the "S1C6200/6200A Core CPU Manual" for transition to the HALT/SLEEP status and timing of its cancellation.

Figures 4.8.2, 4.8.3 and 4.8.4 show the sequence to enter and cancel the SLEEP mode, respectively.

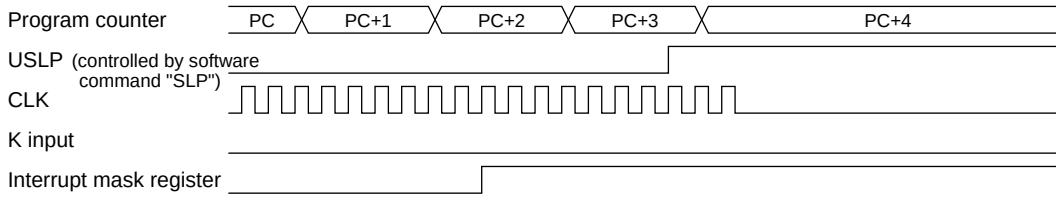


Fig. 4.8.2 Entering SLEEP mode

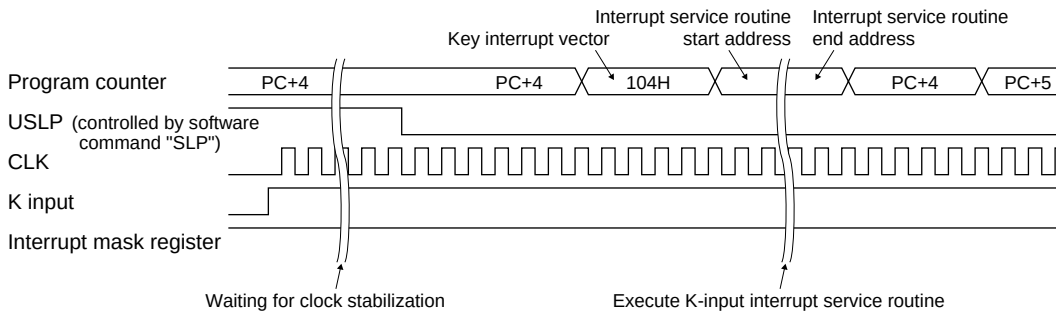


Fig. 4.8.3 Wakeup from SLEEP mode by K-input

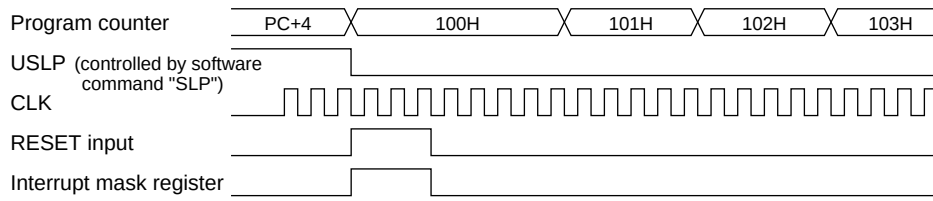


Fig. 4.8.4 Wakeup from SLEEP mode by RESET pad

4.8.1 Interrupt factors

Table 4.8.1.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to 1 depending on the corresponding interrupt factors.
The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to 1.

- The corresponding mask register is 1 (enabled)
- The interrupt flag is 1 (EI)

The interrupt factor flag is a read-only register, but can be reset to 0 when the register data is read.
At initial reset, the interrupt factor flags are reset to 0.

Note: Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Table 4.8.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Clock timer 2 Hz falling edge	IT2 (0EFH•D2)
Clock timer 8 Hz falling edge	IT8 (0EFH•D1)
Clock timer 32 Hz falling edge	IT32 (0EFH•D0)
Input (K00–K03) port rising edge	IK0 (0EDH•D0)

4.8.2 Specific masks for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read / write registers. The interrupts are enabled when 1 is written to them, and masked (interrupt disabled) when 0 is written to them.
At initial reset, the interrupt mask register is set to 0.
Table 4.8.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.8.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT2	(0EBH•D2)	IT2	(0EFH•D2)
EIT8	(0EBH•D1)	IT8	(0EFH•D1)
EIT32	(0EBH•D0)	IT32	(0EFH•D0)
EIK03*	(0E8H•D3)	IK0	(0EDH•D0)
EIK02*	(0E8H•D2)		
EIK01*	(0E8H•D1)		
EIK00*	(0E8H•D0)		

∗ There is an interrupt mask register for each input port pin.

4.8.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU starts interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–07H) to be loaded into the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine).

Note: The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.

Table 4.8.3.1 Interrupt vector addresses

Page	Step	Interrupt vector
1	00H	Initial reset
	01H	Clock timer interrupt
	04H	Input (K00–K03) interrupt
	05H	Clock timer & Input (K00–K03) interrupt

4.8.4 I/O memory of interrupt

Table 4.8.4.1 shows the interrupt control bits and their addresses.

Table 4.8.4.1 Control bits of interrupt

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

EIT32, EIT8, EIT2: Interrupt mask registers (0EBH•D0–D2)
IT32, IT8, IT2: Interrupt factor flags (0EFH•D0–D2)

...See Section 4.7, "Clock Timer".

EIK00–EIK03: Interrupt mask registers (0E8H)
IK0: Interrupt factor flag (0EDH•D0)

...See Section 4.3, "Input Ports".

4.8.5 Programming notes

(1) Restart from the HALT mode is performed by an interrupt. The return address after completion of the interrupt processing will be the address following the HALT instruction.

(2) Restart from the SLEEP mode is performed by an input interrupt from the input port (K00–K03). The return address after completion of the interrupt processing will be the address following the SLP instruction. At least one input port interrupt must be enabled before shifting to the SLEEP mode.

(3) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

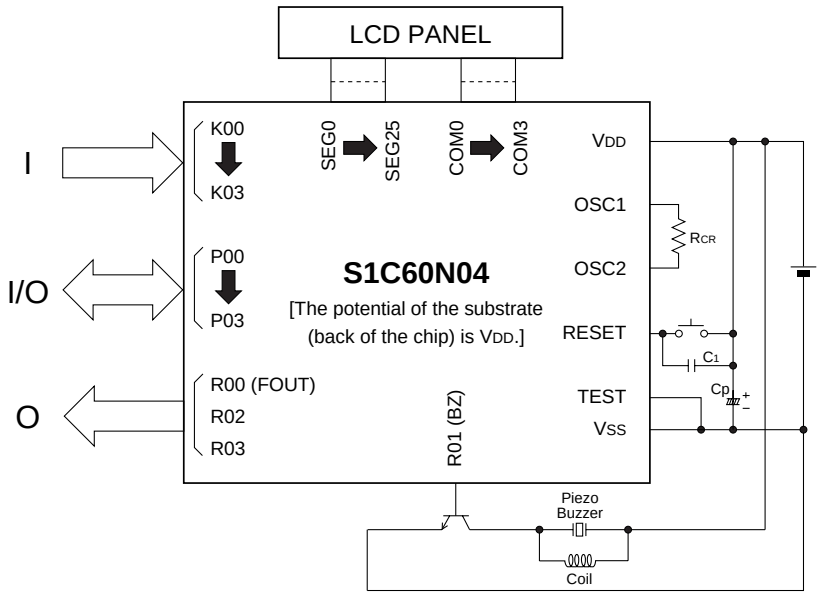
(4) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to 1, the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(5) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

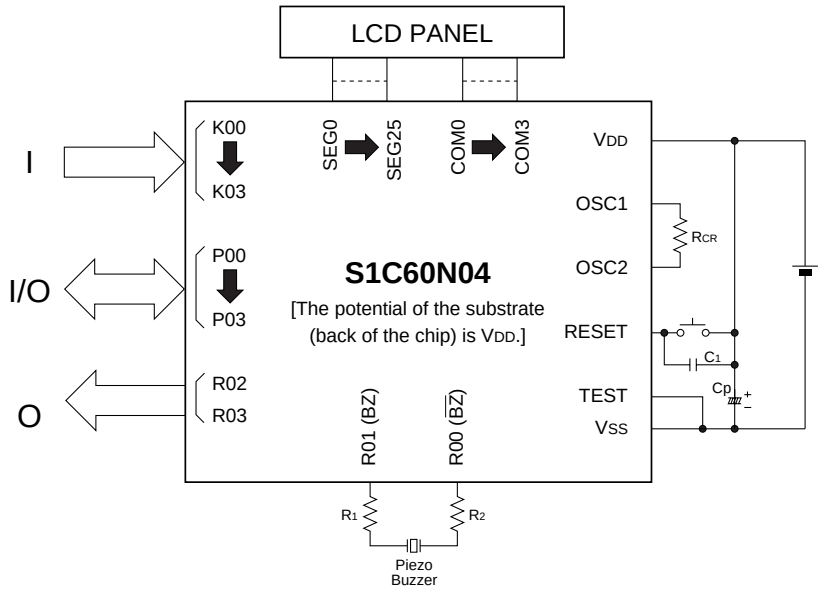
(6) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

Piezo Buzzer Single Terminal Driving



Piezo Buzzer Direct Driving



R_{CR}	Resistor	50 kΩ (V_{SS} = -5.0 V), 39 kΩ (V_{SS} = -3.0 V)
C_1	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF
R_1, R_2	Resistor	100 Ω

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	40	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP12-48pin).

6.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	3 V system, V_{DD}=0V	-3.6	-3.0	-2.7	V
		5 V system, V_{DD}=0V	-5.5	-5.0	-4.5	V
Oscillation frequency	f_{OSC}	CR oscillation, R_{CR}=50kΩ, V_{SS}=-5V		2		MHz

6.3 DC Characteristics

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-5.0V, fosc=2MHz, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull-down	K00–03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, Pull-down	K00–03	20	40	70	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, Pull-down	P00–03, RESET	50	100	150	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, P00–03, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R02, R03, P00–03			-3.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS} (with protection resistor)	R00, R01			-3.0	mA
High level output current (3)	I_{OH3}	V_{OH3}=0.1·V_{SS} , V_{SS}=-4.5V	R03			-15	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R02, R03, P00–03	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS} (with protection resistor)	R00, R01	3.0			mA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–3			-3	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH5}	V_{OH5}=-0.05V	SEG0–25			-3	µA
	I_{OL5}	V_{OL5}=V_{SS}+0.05V		3			µA
Segment output current (during DC output)	I_{OH6}	V_{OH6}=0.1·V_{SS}	SEG0–25			-450	µA
	I_{OL6}	V_{OL6}=0.9·V_{SS}		450			µA

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, fosc=2MHz, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull-down	K00–03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, Pull-down	K00–03	10	25	40	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, Pull-down	P00–03, RESET	30	60	100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, P00–03, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R02, R03, P00–03			-1.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS} (with protection resistor)	R00, R01			-1.0	mA
High level output current (3)	I_{OH3}	V_{OH3}=0.1·V_{SS} , V_{SS}=-2.7V	R03			-5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R02, R03, P00–03	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS} (with protection resistor)	R00, R01	3.0			mA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–3			-3	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH5}	V_{OH5}=-0.05V	SEG0–25			-3	µA
	I_{OL5}	V_{OL5}=V_{SS}+0.05V		3			µA
Segment output current (during DC output)	I_{OH6}	V_{OH6}=0.1·V_{SS}	SEG0–25			-200	µA
	I_{OL6}	V_{OL6}=0.9·V_{SS}		200			µA

6.4 Current Consumption

Unless otherwise specified:
V_{DD}=0V, fosc=2MHz, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{SLP2}	During SLEEP, LCD off	Vss=-3.0V			100	nA
	I_{HALT2}	During HALT, LCD off	no panel load		300	800	µA
	I_{HALT4}	During HALT, LCD on	R_{CR}=39kΩ		330	800	µA
	I_{EXE2}	During operation, LCD off			420	1000	µA
	I_{EXE4}	During operation, LCD on			450	1000	µA
	I_{SLP1}	During SLEEP, LCD off	Vss=-5.0V			100	nA
	I_{HALT1}	During HALT, LCD off	no panel load		950	1500	µA
	I_{HALT3}	During HALT, LCD on	R_{CR}=50kΩ		1000	1500	µA
	I_{EXE1}	During operation, LCD off			1050	1800	µA
	I_{EXE3}	During operation, LCD on			1100	1800	µA

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

CR Oscillation

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-5.0V, R_{CR}=50kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency voltage dispersion	$\Delta f/\Delta V_1$	V_{SS}=-4.5 to -5.5V			20	%
Frequency IC dispersion	$\Delta f/\Delta IC_1$	V_{SS}=-5V	-20	(2MHz)	20	%
Oscillation start time	tsta	V_{SS}=-4.5 to -5.5V		3		mS

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=39kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency voltage dispersion	$\Delta f/\Delta V_2$	V_{SS}=-2.7 to -3.6V			30	%
Frequency IC dispersion	$\Delta f/\Delta IC_2$	V_{SS}=-3V	-20	(2MHz)	20	%
Oscillation start time	tsta	V_{SS}=-2.7 to -3.6V		3		mS

6.6 LCD Characteristic

Unless otherwise specified:
V_{DD}=0V, V_{SS}=V_{L3}, Ta=25°C

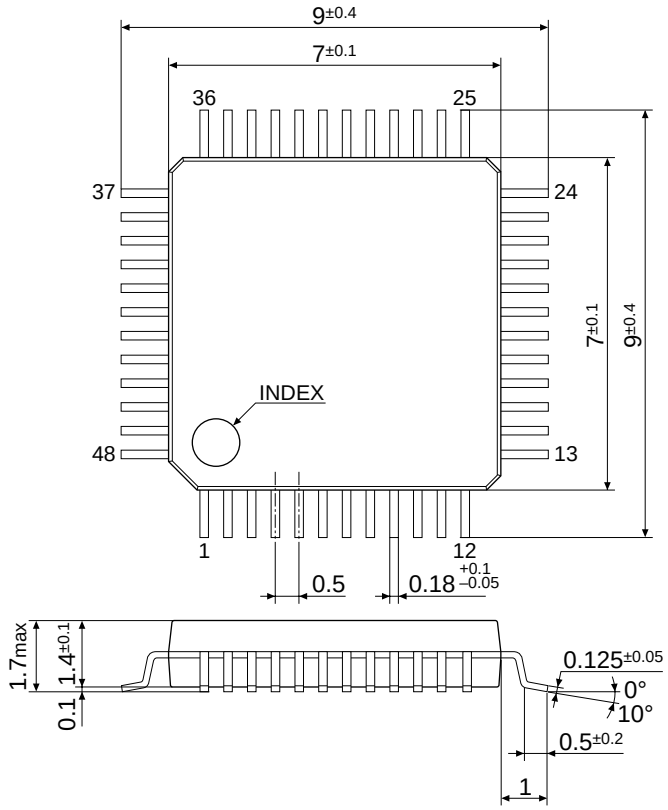
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and common pad (without panel load)	(V_{SS}/3) -0.1	V_{SS}/3	(V_{SS}/3) ×0.9	V

CHAPTER 7 PACKAGE

7.1 Plastic Package

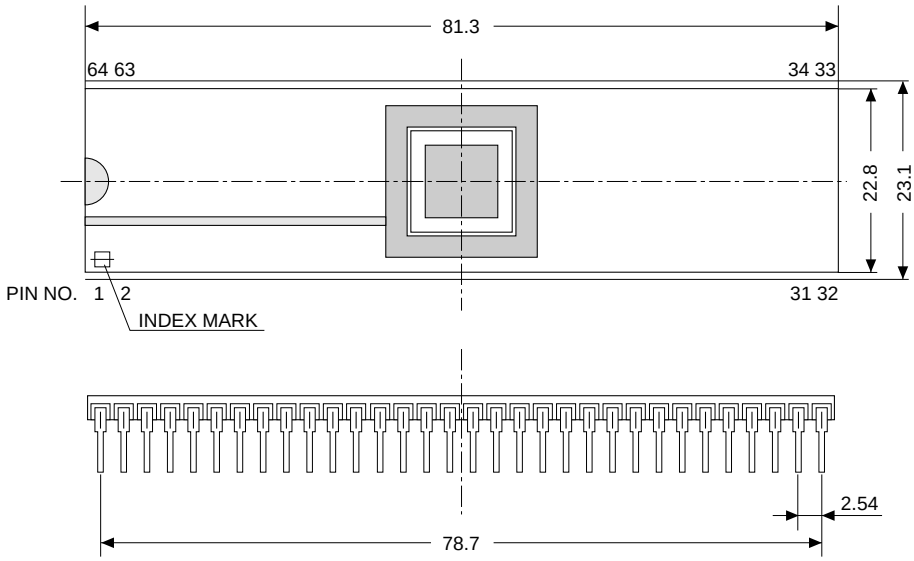
QFP12-48pin

(Unit: mm)



7.2 Ceramic Package for Test Samples

(Unit: mm)

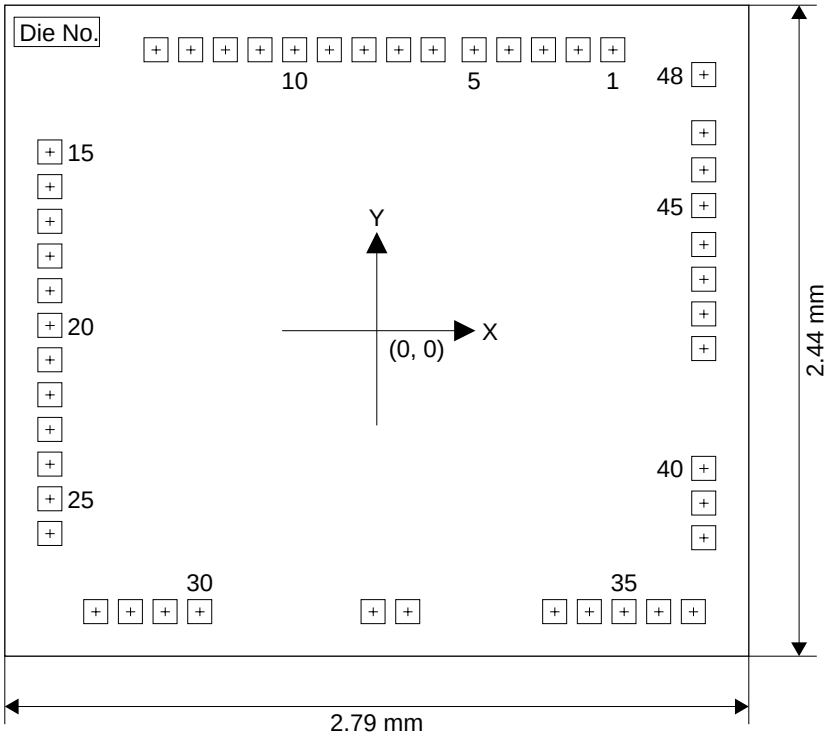


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG5	17	RESET	33	P01	49	SEG18
2	SEG4	18	V_{DD}	34	P00	50	SEG17
3	SEG3	19	OSC1	35	R03	51	SEG16
4	SEG2	20	OSC2	36	R02	52	SEG15
5	SEG1	21	V_{SS}	37	R01	53	SEG14
6	SEG0	22	K03	38	R00	54	SEG13
7	N.C.	23	N.C.	39	N.C.	55	SEG12
8	N.C.	24	N.C.	40	N.C.	56	N.C.
9	N.C.	25	N.C.	41	N.C.	57	N.C.
10	N.C.	26	N.C.	42	SEG25	58	N.C.
11	N.C.	27	N.C.	43	SEG24	59	SEG11
12	COM0	28	K02	44	SEG23	60	SEG10
13	COM1	29	K01	45	SEG22	61	SEG9
14	COM2	30	K00	46	SEG21	62	SEG8
15	COM3	31	P03	47	SEG20	63	SEG7
16	TEST	32	P02	48	SEG19	64	SEG6

N.C. = No Connection

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



8.2 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG25	885	1053	17	SEG9	-1226	410	33	VDD	667	-1053
2	SEG24	755	1053	18	SEG8	-1226	280	34	OSC1	797	-1053
3	SEG23	625	1053	19	SEG7	-1226	150	35	OSC2	927	-1053
4	SEG22	495	1053	20	SEG6	-1226	20	36	VSS	1057	-1053
5	SEG21	365	1053	21	SEG5	-1226	-109	37	K03	1187	-1053
6	SEG20	211	1053	22	SEG4	-1226	-240	38	K02	1226	-776
7	SEG19	82	1053	23	SEG3	-1226	-370	39	K01	1226	-646
8	SEG18	-48	1053	24	SEG2	-1226	-500	40	K00	1226	-516
9	SEG17	-178	1053	25	SEG1	-1226	-630	41	P03	1226	-67
10	SEG16	-308	1053	26	SEG0	-1226	-760	42	P02	1226	63
11	SEG15	-438	1053	27	COM0	-1054	-1053	43	P01	1226	193
12	SEG14	-568	1053	28	COM1	-924	-1053	44	P00	1226	323
13	SEG13	-698	1053	29	COM2	-794	-1053	45	R03	1226	469
14	SEG12	-828	1053	30	COM3	-664	-1053	46	R02	1226	603
15	SEG11	-1226	670	31	TEST	-14	-1053	47	R01	1226	742
16	SEG10	-1226	540	32	RESET	116	-1053	48	R00	1226	960

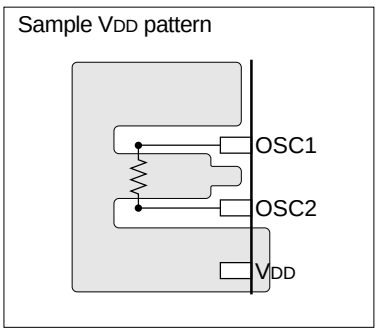
CHAPTER 9 PRECAUTIONS ON MOUNTING

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1 and OSC2 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VDD pattern as large as possible at circumscription of the OSC1 and OSC2 terminals and the components connected to these terminals. Furthermore, do not use this VDD pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and VSS, please keep enough distance between OSC1 and VSS or other signals on the board pattern.

<Reset Circuit>

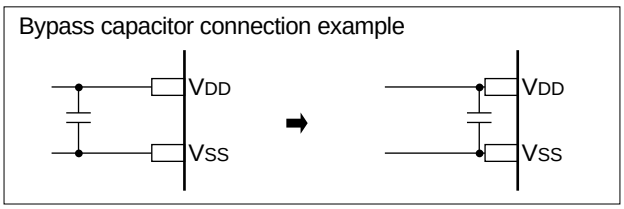
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

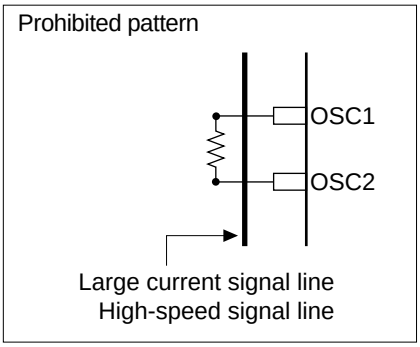
  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

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